CYSEC Cybersecurity TU Darmstadt | System Security Lab | TECHNISCHE UNIVERSITÄT DARMSTADT

HiWi Position – FPGA-based Prototyping of Security Architectures

Background

Hardware-assisted security mechanisms are becoming increasingly important now as software-only defenses are failing against both software-based attacks and the imminent rise of hardware-based attacks. Hardware-assisted security can provide security at reduced overhead, increased efficiency and with stronger guarantees against a wider range of adversaries. One such project involves architecting new attestation protocols to verify the integrity of code both statically and dynamically at runtime. We aim to extend an open-source processor with attestation and other security mechanisms and evaluate their performance, security guarantee and efficiency.

Tasks

The tasks required involve implementing basic digital design and controllers to enable hardware-assisted security mechanisms and processor extensions. An open-source processor would then be extended with this logic, simulated, and synthesized. Evaluation of cost and performance of different mechanisms is also required. Prototyping on FPGA and with different open-sources processors would also be expected.

Position

- Available immediately
- Duration: 3-months, extendable

Requirements

- Verilog and/or VHDL knowledge and basic digital design and integration
- Hands-on FPGA experience
- Familiar with Xilinx Vivado Synthesis toolchain and RTL simulation
- Familiar with basics of processor design
- Familiar with embedded and integrated systems architecture

Contact

Please send your application (incl. CV and certificate(s)) via email to:
Ghada Dessouky
ghada.dessouky@trust.tu-darmstadt.de
or
Shaza Zeitouni
shaza.zeitouni@trust.tu-darmstadt.de

AK Professor Dr.-Ing. Ahmad-Reza Sadeghi
Gebäude S4|14 (CASED Gebäude)
Mornewegstraße 30
64293 Darmstadt
https://www.trust.informatik.tu-darmstadt.de

July 2016